Highly efficient, very compact GaAs power module for cellular telephone

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ABSTRACT

A power module with high efficiency and small size has been developed for cellular telephones. The module, which is composed of a 2-stage amplifier with GaAs MESFETs and packaged into a very small volume of 0.8 cc, shows excellent RF characteristics of the output power P_{out} = 32.3 dBm and the power-added efficiency η add = 65 % at f = 930 MHz, P_{in} = 7 dBm, V_{dd} = 4.7 V. This power module has contributed to realization of compact cellular telephone.

INTRODUCTION

Demands for low-voltage operation and small size in cellular telephones have been increasing dramatically in recent years. A power amplifier module is one of the most important devices in cellular phones [1]. The improvement of the electrical characteristics and the size minimization of the power module enormously contribute to the extension of the operating time and the size reduction of the phone. For this purpose, we have made the following improvements:

1) development of high performance GaAs MESFETs.

2) establishment of circuit design suitable for a module.

3) achievement of very high-density assembly.

In this paper, we report on design, fabrication methods and performances of the newly-developed power module and GaAs MESFETs.

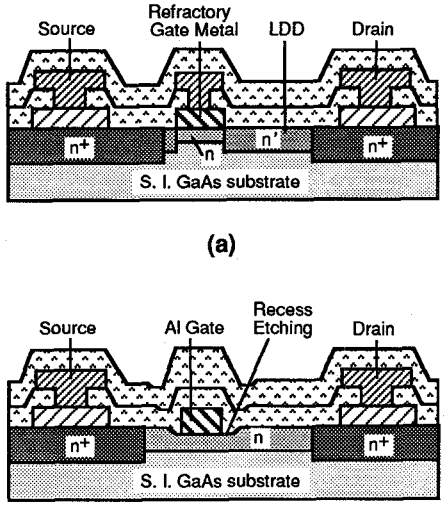

Figure 1 Cross-sectional views of GaAs power MESFETs, (a) the 1st FET with refractory gate and (b) the 2nd with Al gate.

MESFET DESIGN AND CHARACTERISTICS

Figure 1 (a) and (b) show cross-sectional views of the 1st-stage FET and 2nd-stage FET used in the module, respectively. The offset gate and LDD (Lightly Doped Drain) structure with refractory gate metal [2] was applied to the 1st FET to obtain a high power gain, and the offset gate and recess etching structure with Al gate to the 2nd FET to obtain a high breakdown voltage. Photographs of these FETs are shown in Figure 2 (a) and (b), where the chip size of the 1st FET is 0.55 mm x 0.6 mm, that of the 2nd FET is 0.55 x 2.0 mm.

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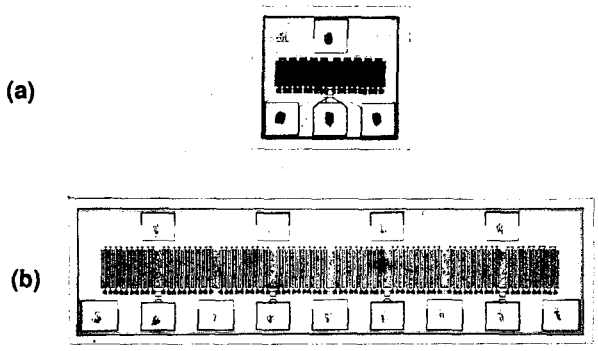

Figure 2 Microscope photographs of MESFETs, (a) the 1st FET with 0.55 mm x 0.6 mm chip size and (b) the 2nd with 0.55 mm x 2.0 mm.

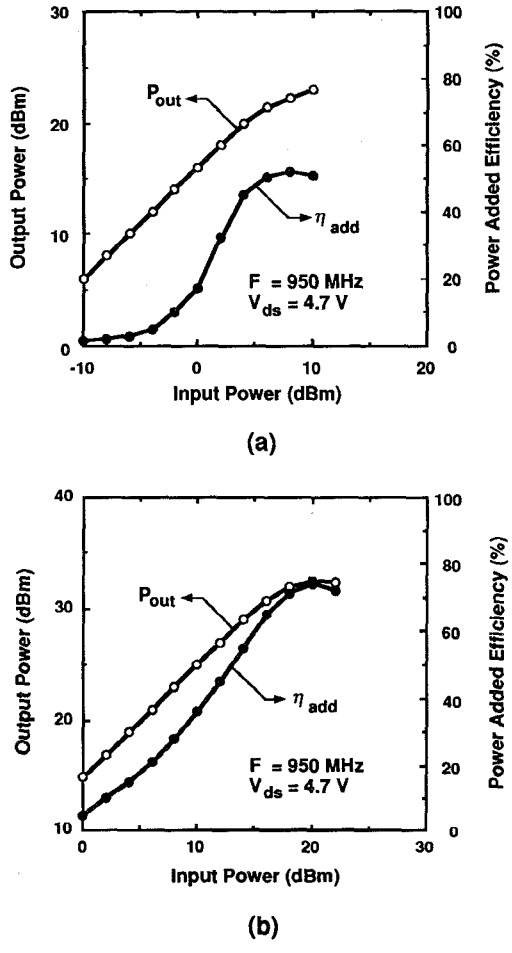

Figure 3 Output power and power-added efficiency versus input power, (a) the 1st FET properties of class A operation and (b) the 2nd of class B.

These FETs were optimized for the following parameters: gate length, finger length, gate width and threshold voltage to realize the high efficiency and low-voltage operation. As a result, high output power P_{out} and power-added efficiency η_{add} have been obtained. Figure 3 (a) and (b) show dependencies of P_{out} and η_{add} on input power P_{in} of the 1st and the 2nd FET, where the operating conditions are as follows, frequency f = 950 MHz and drain-to-source bias voltage V_{ds} = 4.7 V. The typical RF data of the 1st FET are P_{out} = 22 dBm, η_{add} = 50 % (Pin = 7 dBm, class A operation), and those of the 2nd FET are P_{out} = 32.5 dBm, η_{add} = 75 % (P_{in} = 20 dBm, class B operation).

MODULE DESIGN AND PERFORMANCES

Figure 4 shows an equivalent circuit of the power module. The module is comprised of the 1st and 2nd FETs and impedance matching circuits. The drain bias voltages are supplied by λ/4 microstrip lines and the gate bias voltages by bleeder resistors. The 2nd and the 3rd harmonics absorption circuits are formed on the output side of the 2nd FET.

Figure 5 shows P_{out} and η_{add} versus a load impedance of the 1st FET, where the bias conditions are f = 950 MHz, V_{ds} = 4.7 V and P_{in} = 7 dBm. The solid lines on Figure 5 indicate simulated values using a nonlinear circuit model, and the circles experimental results, respectively. In the design of this module, the load impedance of the 1st FET has been set a 50 Ω.

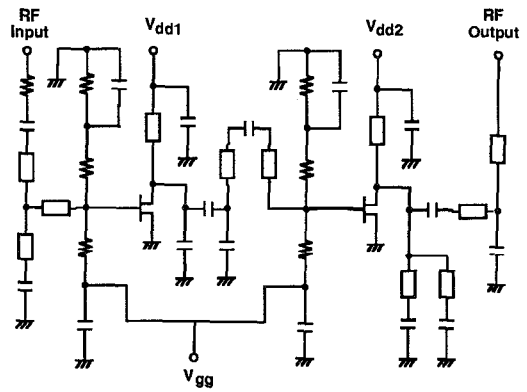

Figure 4 Equivalent circuit of a power module composed of a 2-stage amplifier.

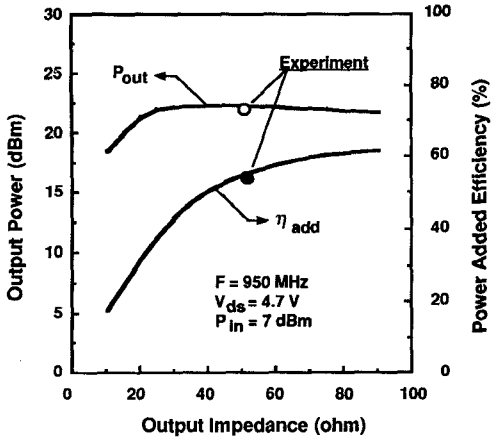

Figure 5 Simulated (lines) and experimental (circles) values of output power and power-added efficiency versus load impedance of the 1st FET.

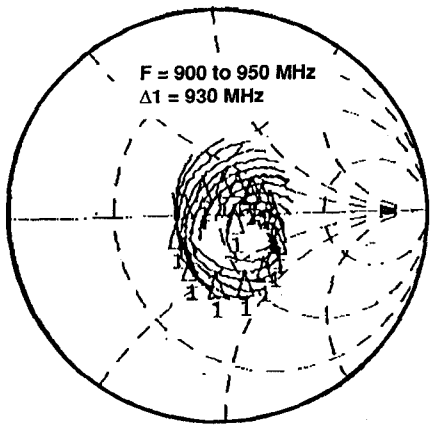

Figure 6 Stability of the load impedance of the 1st FET, while that of the 2nd changes according to : VSWR = 5, All Phase Angles.

This serves to simplify the circuit design and the evaluation of the module, and consequently to improve the stability of the module. Figure 6 shows changes of the load impedance of the 1st FET when the load of the module changes according to : VSWR = 5, all phase angles. Although the 1st FET has an oscillation region at one part of VSWR = 4, the load impedance of the 1st FET in the module rotates around 50 Ω (VSWR < 2). The 1st FET is completely stable even when the output impedance of the module changes largely. This stability contributes to the anti-oscillation property of the module.

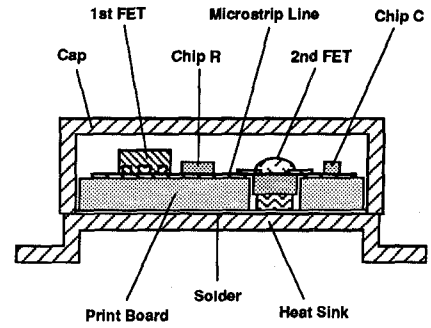

Figure 7 Cross-sectional view of the power module.

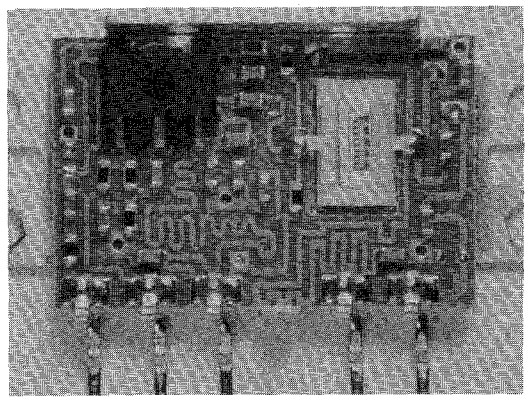

Figure 8 Top view photograph of the power module with 0.8 cc in size.

To realize high-density assembly, a semi-flexible print board and new chip resistors and capacitors of 1.0 mm x 0.5 mm in size (1005-type) have been used. Figure 7 shows a cross-sectional view of the power module, where the print board is made of PPO (poly-Phenylene Oxide) with low dielectric tangent (tan δ = 0.003) and high dielectric constant (ε_r = 10.5). Microstrip lines on the board are formed by using Cu metal. The 1st FET assembled on a surface type package and chip C/Rs are mounted on the print board. The back surface of the 2nd FET assembled on a ceramic/metal type package is soldered on a heat sink of the module frame directly. The top view photograph of the module is shown in Figure 8. The gate bias voltages of the 1st and 2nd FETs are supplied from one terminal of the module. The gate leads of both FETs are connected to each other inside the module by using a through hole and a back surface pattern on the print board. As the 1st FET is molded on a surface mount type package, the print board area under the 1st FET

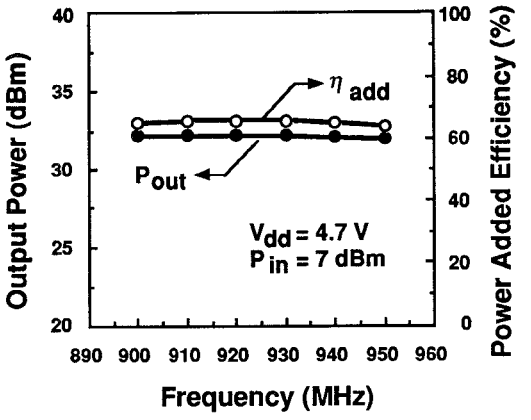

Figure 9 Dependence of output power and power-added efficiency on frequency of the module.

contributes to the internal matching circuit for it. Owing to these technologies, the entire circuit (matching circuits and harmonics absorption circuits) can be formed on a 10.5 mm x 16 mm size print board. The total size of the module becomes 12 mm x 17 mm x 4 mm (0.8 cc).

Figure 9 shows P_{out} and η_{add} dependence on frequency of the module at an operating voltage V_{dd} = 4.7 V. In the 50 MHz band width from 900 to 950 MHz, fairly flat properties of P_{out} and η_{add} have been obtained. The RF characteristics of the module are following : P_{out} = 32.3 dBm and η_{add} = 65 % at f = 930 MHz, P_{in} = 7 dBm, V_{dd} = 4.7 V and V_{gg} = -3.5 V, as shown in Table 1.

CONCLUSION

A highly efficient and very compact power module using GaAs MESFETs has been developed for cellular telephone. The very-high performance FETs, PPO print board and 1005-type chip C/Rs are mounted inside of very small frame of 0.8 cc. The load impedance of the 1st FET in the module is set at 50 Ω in order to satisfy the stability of the module to prevent oscillation. The typical RF properties of the module are as follows, P_{out} = 32.3 dBm and η_{add} = 65 % at f = 930 MHz, P_{in} = 7 dBm, V_{dd} = 4.7 V. This module has contributed to expanding of the communication time of the cellular telephone drastically.

TABLE 1 Characteristics of the newly developed power module.

Print Board Size :		10.5 mm x 16 mm
Casing Size	:	12 mm x 17 mm
Chip C/R Size	:	1.0 mm x 0.5 mm
Number of C	:	16
Number of R	:	8
Volume	:	0.8 cc
Frequency	:	930 MHz
Vdd1, Vdd2	:	4.7 V
Vgg	:	-3.5 V
Input Power	:	7.0 dBm
Output Power	:	32.3 dBm
Total Efficiency	:	65 %

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